Verification of Translation

U.S. Patent Application No. 10/756,961
Title of the Invention:

SEMICONDUCTOR MEMORY DEVCE WITH TRENCH-TYPE STACKED CELL CAPACITORS AND METHOD FOR MANUFACTURING THE SAME

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At Osaka, Japan
DATED this May 15, 2006

Signature of the translator Yoko Yasuda.

Yoko YASUDA

JAPAN PATENT OFFICE

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[Document Name] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR MEMORY DEVCE

[Claims]

[Claim 1] A semiconductor device comprising:

a storage capacity element portion comprising many capacitors with the same shape,

wherein an interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are buried to form the capacitors, and

any capacitor is arranged so that only a part of a side face of one trench is opposite to that of the other.

[Claim 2] A semiconductor device comprising:

a storage capacity element portion comprising many capacitors with the same shape,

wherein an interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are buried to form the capacitors, and

any capacitor is arranged so that a side face of one trench is opposite completely to that of the other, and has a shape in which a distance between the opposing side faces is larger at central portions of the respective trenches.

[Claim 3] A semiconductor device comprising:

a storage capacity element portion comprising many capacitors with the same shape,

wherein an interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are buried to form the capacitors, and

a concavity is provided between the adjacent cell capacitors and the plate electrode is buried in the concavity.

[Claim 4] The semiconductor device according to any one of claims 1, 2, or 3, wherein a relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a semiconductor memory device, in particular, a dynamic random access memory (i.e., DRAM) whose memory cell portion has a trench-type stacked cell structure. More specifically, the present invention relates to a semiconductor memory device including a storage capacity element portion that is suitable for a highly integrated device and has high reliability.

[0002]

[Prior Art]

With the implementation of a smaller-scale device and a larger-capacity DRAM in recent years, the surface area occupied by a single memory cell on a chip of a semiconductor memory device is reduced increasingly.

[0003]

FIG. 6 is a top view showing trench-type stacked cell capacitors (i.e., concave-type capacitors) formed in a memory cell region. FIG. 7 is a cross-sectional view taken along the line I–II in FIG. 6. FIG. 7 illustrates cell capacitors A, B and C that are adjacent to one another. Each of the cell capacitors is a trench-type stacked cell, i.e., the cell capacitor region is recessed, and the plate electrode 110 is exposed on the entire surface.

These cell capacitors are connected to transfer transistors so as to form a storage capacity element portion (i.e., a DRAM circuit), as shown in FIG. 8.

[0004]

The following is an explanation of the structure shown in FIG. 7. An interlayer insulating film 111 is deposited on the region where memory cells are formed. The interlayer insulating film 111 has holes for providing storage nodes (i.e., lower electrodes of the memory cells), and conductive films 108 that act as the storage nodes are formed in the holes. Each of the storage nodes is connected to a plug 112 via a barrier metal (not shown). A capacitor insulating film 109 and the plate electrode 110 are deposited on the entire surface, including the insides of the holes where the storage nodes have been formed, without removing the interlayer insulating film 111. In other words, the trench-type stacked cell structure is a cell structure that utilizes only the inner surfaces of the trenches defined by the interlayer insulating film as capacitors.

[0005] The manufacturing process of the trench-type stacked cell structure is simple because it eliminates the removal of the interlayer insulating film and can proceed to the next step. Moreover, it is not necessary to estimate a margin between cell capacitors when the cell capacitor pattern is formed by lithography and dry etching. Thus, the manufacturing process is very effective in scaling down the device. A large-capacity DRAM can be achieved by arranging a number of small trench-type stacked cells that are produced in such a simple process as described above.

[0006]

In view of this, the trench-type stacked cell structures shown in FIGS. 6 and 7 are expected to be used as the capacitor structure of memory cells in a future DRAM.

[0007]

[Problems to be solved by the Invention]

In this structure, though the storage nodes (i.e., the lower electrodes) of the individual cell capacitors are separated electrically and have different potentials, an interlayer insulating film is interposed between the adjacent cell capacitors. Therefore, there is a problem of the generation of a parasitic capacitance.

[0008]

For instance, in the example shown in FIG. 7, the interlayer insulating film 111 is interposed between the storage node 108a of the cell capacitor A and the storage node 108b of the cell capacitor B. Thus, a parasitic capacitance C_{p4} is generated between the cell capacitors so as to make a connection between them, as indicated by the broken line in FIG. 8.

[0009]

FIG. 9 is a cross-sectional view showing the structure of simple-stacked memory cells. In FIG. 9, capacitor insulating films 102, and thereon a plate electrode 103 are formed so as to cover cylindrical storage nodes 101. FIG. 10 is a cross-sectional view showing the structure of cylindrical cell capacitors. In FIG. 10, capacitor insulating films 105, and thereon a plate electrode 106 are formed so as to cover the inner and outer surfaces of cylindrical storage nodes 104. For the structures as shown in FIGS. 9 and 10, the adjacent cell capacitors are connected electrically by the plate electrodes 103 and 106, respectively, each of which has the same electric potential. Therefore, a large parasitic capacitance is not generated between the adjacent cell capacitors even if the plate electrode is covered with an interlayer insulating film (not shown).

[0010]

Compared with other cell structures, the trench-type stacked cell structure is likely to generate a larger parasitic capacitance even if the distance between adjacent cell capacitors is the same. The effect of the parasitic capacitance on the operation of a DRAM circuit will be described in detail later.

[0011]

With the foregoing in mind, it is an object of the present invention to reduce a parasitic capacitance in a semiconductor device that uses a trench-type stacked cell structure in the DRAM memory cell region.

[0012]

[Means for Solving the Problems]

A first semiconductor device of the present invention includes a storage capacity element portion including many capacitors with the same shape. An interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are buried to form the capacitors. Any capacitor is arranged so that only a part of a side face of one trench is opposite to that of the other.

[0013]

In the first semiconductor device of the present invention, unlike the conventional technique, the side face of one capacitor is not opposite completely to that of the other. Therefore, the parasitic capacitance can be reduced.

[0014]

A second semiconductor device of the present invention includes a storage capacity element portion including many capacitors with the same shape. An interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are

buried to form the capacitors. Any capacitor is arranged so that a side face of one trench is opposite completely to that of the other, and has a shape in which the distance between the opposing side faces is larger at the central portions of the respective trenches.

[0015]

In the second semiconductor device of the present invention, the distance between the opposing side faces of the capacitors is not constant but is increased partially. Therefore, even if the side face of one capacitor is opposite completely to that of the other, the parasitic capacitance can be reduced.

[0016]

A third semiconductor device of the present invention includes a storage capacity element portion including many capacitors with the same shape. An interlayer insulating film has a plurality of trenches, in each of which a storage node, a capacitor insulating film, and a plate electrode are buried to form the capacitors. A concavity is provided between the adjacent cell capacitors and the plate electrode is buried in the concavity.

[0017]

In the third semiconductor device of the present invention, the potential is fixed by the plate electrode in the region where the storage nodes of the adjacent capacitors are buried. Therefore, the parasitic capacitance is not generated in the region where the plate electrode is buried, so that the parasitic capacitance can be reduced.

[0018]

In the first to third semiconductor device of the present invention, it is preferable that the relative dielectric constant of the interlayer insulating film is smaller than that of a silicon oxide film. The use of a low dielectric

constant film as the interlayer insulating film can further reduce the parasitic capacitance.

[0019]

[Embodiments of the Invention]

Effect of Parasitic Capacitance

The effect of an increase in parasitic capacitance between the adjacent cells will be described in detail by referring to FIG. 8. FIG. 8 is a circuit diagram of a DRAM. Reference numeral C_{S1} denotes a capacitance of a cell capacitor A, C_{S2} denotes a capacitance of a cell capacitor B, and C_p denotes a parasitic capacitance.

[0020]

When one of the adjacent memory cell capacitors A and B, e.g., the capacitor A is in the charge storage state ("1") and the capacitor B is in the discharge state ("0"), the parasitic capacitance C_p has the following effect on both capacitors. With an increase in the parasitic capacitance C_p, the potential of the capacitor B in the discharge state is increased as a result of being affected by the potential of the capacitor A in the charge storage state, while the potential of the capacitor A is decreased as a result of being affected by the potential of the capacitor B.

[0021]

When reading is performed after charge has been retained in the above condition, information that has been originally in the discharge or charge storage state exceeds the threshold voltage for discriminating between the two states. Consequently, the cell capacitor in its discharge state is recognized as to be in the charge storage state or the cell capacitor in its charge storage state is recognized as to be in the discharge state. Thus, the information is detected as an error signal, which prevents normal

operation of the memory.

[0022]

First Embodiment

A first embodiment of the present invention devices the arrangement (i.e., the layout) of memory cells in a cell capacitor array to reduce the parasitic capacitance.

[0023]

FIG. 1 is a plan (top) view showing the layout of a memory cell capacitor array in a storage capacity element portion of the present invention. The shape of each cell capacitor is indicated by a broken line. In general, the shape is rectangular (square) when patterned by lithography. However, the actual cell capacitor has four rounded corners due to etching or the like, and finally is in the form of a rectangle with four rounded corners, such as a cell shown in FIG. 1, or close to an ellipse.

[0024]

Unlike a conventional layout in which the adjacent cell capacitors are opposite completely to each other, this embodiment is characterized by a layout in which the adjacent cell capacitors are staggered so that only a part of a side face of one cell capacitor is opposite to that of the other. FIG. 2 is a cross-sectional view showing the structure of the cell capacitors, taken along the line I–II in FIG. 1. In FIG. 2, reference numeral 11 denotes an interlayer insulating film, 8 denotes storage nodes, 9 denotes a capacitor insulating film, 10 denotes a plate electrode, and 12 denotes plugs. In the layout of FIG. 2, only the cell capacitors A and C are illustrated, and the cell capacitor B that should be located between them is not described. However, the cell capacitor B will be present in the cross-sectional view taken along the line III–IV in FIG. 1, like the conventional example shown in FIG. 7.

[0025]

An aspect of this embodiment is modification in the layout of cell capacitors. While the opposing side faces of adjacent cell capacitors are opposite completely to each other in the conventional layout, this embodiment allows only a part of a side face of one cell capacitor to be opposite to that of the other. This layout can provide at least a cross section of the cell array that does not include a cell capacitor that would have been present as one of the adjacent cell capacitors in the conventional layout. Thus, the parasitic capacitance can be reduced.

[0026]

Here, using numerical examples, the parasitic capacitance of this embodiment is compared with that of the conventional cell layout.

[0027]

First, the parasitic capacitance value in the conventional layout is estimated with reference to FIGS. 6 and 7. FIG. 6 shows the planar layout of a conventional memory cell capacitor array, and FIG. 7 is a cross-sectional view showing the structure thereof. It should be noted that the following values are only an example for explaining the effects of the present invention and those values may be changed appropriately as needed.

[0028]

A set cell capacitance value is expressed by

$$C_{s1} = \varepsilon_0 \times \varepsilon_2 \times 2 \times (L_{s1} + L_{s2}) \times H \div d \qquad (1)$$

where ε_0 is a dielectric constant in vacuum, L_{s1} is the short side length of a cell capacitor, L_{s2} is the long side length of the cell capacitor, H is the height of the cell capacitor, d is the thickness of a capacitor insulating film (i.e., the

thickness converted to a silicon oxide film), and ε_2 is a relative dielectric constant of the silicon oxide film. With the substitution of $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m, $L_{s1} = 0.15$ μm, $L_{s2} = 0.8$ μm, $H = 3$ μm, $d = 5.0$ nm, and $\varepsilon_2 = 3.9$, Equation (1) yields 15 fF per cell capacitor.

[0029]

When cells in the above-described form are arranged geometrically so that each of them is aligned with the adjacent cells in both the vertical and horizontal directions as shown in FIG. 6, the parasitic capacitance C_{p4} is expressed by

$$C_{p4} = \varepsilon_0 \times \varepsilon_1 \times L_{s2} \times H \div T_{s1} \qquad (2)$$

where ε_1 is a relative dielectric constant of the interlayer insulating film and T_{s1} is the distance between the cell capacitors A and B. Substitution of $T_{s1} = 0.08$ μm into Equation (2) yields the parasitic capacitance C_{p4} of about 0.8 fF. This value reaches as much as 5.3% (calculated by $0.8 \div 15 \times 100$) of the set cell capacitance value (15 fF).

[0030]

The operation of memory cells when the parasitic capacitance value is not less than 5% of the cell capacitance value will be described with reference to FIG. 8. For example, when data of logic level "High" is written onto the cell capacitor B while the cell capacitors A and B have been in the logic level "Low" state, i.e., in the discharge state, the word line WL2 is activated to apply a voltage that is supplied as the potential of a bit line BL1. At this time, a potential difference $V_p - V_d$ between the voltage V_p of the plate electrode and the step-up voltage V_d (i.e. the potential of BL1) is applied to the cell capacitor B, so that charge is accumulated.

[0031]

However, in the case where the parasitic capacitance is present between the cell capacitors A and B and between the cell capacitors C and B, the cell capacitors A and C are connected in parallel when viewed from the cell capacitor B. As is generally known, the capacitance of the parallel-connected capacitors is determined by adding their capacitances. In this case, the capacitance of $2C_{p4} = C_{p4} + C_{p4}$ is connected in series with the cell capacitor B.

[0032]

When the cell capacitors A and C are in the logic level "Low" state, the potential difference is applied under the condition that the parasitic capacitance $2C_{p4}$ is connected in series with the cell capacitance C_{s2} of the cell capacitor B. Assuming that the parasitic capacitance C_{p4} is 5% of the cell capacitance C_{s2}, the potential applied to a target cell causes 5% loss compared with the original potential to be applied. When another cell capacitor in the same logic state is present in the opposite direction to the target cell, the potential causes as much as 10% loss in total.

[0033]

In general cell structure design, a margin for an applied voltage and an operating voltage is set to a maximum of 10%. When the parasitic capacitance is more than 10%, it exceeds the set margin. Consequently, writing operation cannot be ensured. Therefore, both the expected charge retention amount and charge retention time as the basic performance of memory cells cannot be ensured due to the parasitic capacitance.

[0034]

Even when data is read out of a cell capacitor in the charge retention state, the cell capacitor is recognized as to be in the discharge state because

the potential difference for reading has been lowered by the parasitic capacitance.

[0035]

As shown in FIG. 1, when the adjacent cell capacitors are staggered so that only a part of a side face of one cell capacitor is opposite to that of the other instead of arranging them to be opposite completely to each other like the conventional layout, the parasitic capacitance C_{p1} is expressed by

$$C_{p1} = \varepsilon_0 \times \varepsilon_1 \times L_d \times H \div T_{s1} \qquad (3)$$

where L_d is the length of a portion where the opposing cell capacitors are overlapped. Substitution of $L_d = 0.6$ μm into Equation (3) yields $C_{p1} = 0.6$ fF, which is 4% (calculated by $0.6 \div 15 \times 100$) of the set cell capacitance value (15fF).

[0036]

In the pattern layout of this embodiment, the adjacent cell capacitors are not opposite completely, but are opposite partially to each other. Thus, a difference in the parasitic capacitance between the layout of this embodiment and that of the conventional example is given by

$$\Delta C_{p1} = C_{p4} - C_{p1}, \qquad (4)$$

showing that the parasitic capacitance can be reduced by 1.3%. The above equations (1) to (4) are used to calculate only the capacitance between adjacent cells, which exerts the greatest effect on the parasitic capacitance, and ignores the parasitic capacitance effected by other cells.

[0037]

This embodiment can reduce the parasitic capacitance by providing the cell layout as described above, even if the cell size and the capacitor size are the same as those of a conventional example.

[0038]

It is preferable to set an amount by which the adjacent capacitors overlap in the mask layout so that the parasitic capacitance between the adjacent capacitors is not more than 10% of the accumulated charge capacitance for each capacitor. This is because malfunction occurs remarkably when the parasitic capacitance is more than 10% of the set capacitance.

[0039]

The above method makes it possible to reduce the parasitic capacitance between the adjacent capacitors and suppress a signal error caused by noise without changing the conventional capacitor shape, capacitance, or the like.

[0040]

Second Embodiment

A second embodiment of the present invention devices the shape of a cell capacitor, which will be described with reference to FIG. 3.

[0041]

FIG. 3 shows a planar layout of memory cell capacitors in a semiconductor memory device of this embodiment. Each cell capacitor is not simply rectangular, but has such a shape that the central portions of its long sides are recessed, and the distance between those central portions of the respective side faces of the opposing cells is larger.

[0042]

FIG. 4 is a cross-sectional view showing the structure of the cell

capacitors, taken along the line V–VI in FIG. 3. As shown in FIG. 4, the width of the interlayer insulating film between the cell capacitors is decreased partially. In FIG. 4, reference numeral 11 denotes an interlayer insulating film, 8 denotes storage nodes, 9 denotes a capacitor insulating film, 10 denotes a plate electrode, and 12 denotes plugs.

[0043]

When the cell capacitors have the shape illustrated in FIGS. 3 and 4, the distance between the recessed portions of the cell capacitors is given by $L_{s3} + T_{s1} + L_{s3}$. This makes the distance between the central portions of the opposing cell capacitors larger. Therefore, even if the cell capacitors are arranged orderly in both the vertical and horizontal directions so that the side face of one cell capacitor is opposite completely to that of the other like the conventional cell capacitors, the parasitic capacitance can be reduced as a whole.

[0044]

When each of adjacent cell capacitors has recessed portions in its long sides in the direction in which the parasitic capacitance value is increased, the parasitic capacitance is expressed by

$$C_{p2} = \varepsilon_0 \times \varepsilon_1 \times \{(L_{s2} - L_{s4}) \times H \div T_{s1} + (L_{s4} \times H \div (L_{s3} + T_{s1} + L_{s3}))\} \quad (5)$$

where L_{s3} is the length of the recessed portion in the short side direction and L_{s4} is the length of the recessed portion in the long side direction. In this case, a difference in the parasitic capacitance that is generated between cells having no recessed portion and between cells having recessed portions is given by

$$\Delta C_{p2} = C_{p4} - C_{p2} \qquad (6).$$

[0045]

Using specific values in the conventional example, when $L_{s3} = 0.03$ μm and $L_{s4} = 0.4$ μm, ΔC_{p2} is 0.57 fF. This is 3.8% (calculated by $0.65 \div 15 \times 100$) of the individual set cell capacitance value (15fF). Accordingly, the parasitic capacitance, which is generated between a target capacitor and the capacitor adjacent to one side of the target capacitor, can be reduced by 1.5%.

[0046]

In this embodiment, each cell capacitor is provided with recessed portions having straight sides and square corners so as to increase the distance between the central portions of the opposing side faces. However, the same effect can be obtained by recessed portions having a curved shape with a curvature.

[0047]

This embodiment can reduce the parasitic capacitance by forming the cells as described above, even if the cell layout is the same as that of a conventional example.

[0048]

It is preferable to modify the cell shape so that the parasitic capacitance between the adjacent capacitors is not more than 10% of the accumulated charge capacitance for each capacitor. This is because malfunction occurs remarkably when the parasitic capacitance is more than 10% of the set capacitance.

[0049]

The above method also makes it possible to reduce the parasitic capacitance between the adjacent capacitors and suppress a signal error caused by noise without changing the conventional cell layout, capacitance,

or the like.

[0050]

Third Embodiment

A third embodiment of the present invention reduces the parasitic capacitance in such a manner that a concavity is formed in the upper portion of an interlayer insulating film between cell capacitors and a plate electrode is buried in the concavity.

[0051]

This embodiment will be described with reference to FIG. 5. FIG. 5 is a cross-sectional view of the memory cell capacitors in a semiconductor memory device of this embodiment. These cell capacitors are arranged in the same manner as the conventional example shown in FIG. 6, and the cross section is taken along the line I–II of FIG. 6.

[0052]

This embodiment is the same as the conventional example in that storage nodes 8 and a capacitor insulating film 9 are buried in the trenches formed in an interlayer insulating film 11. The structure of the semiconductor device of this embodiment differs from the conventional example in that a plate electrode 20 is buried in concavities (20a and 20b) provided between the cell capacitors.

[0053]

When the plate electrode 20 is buried in the concavity between the cell capacitors, the potential in the region between the adjacent cell capacitors where the plate electrode is buried is fixed due to the buried plate electrode. Therefore, the parasitic capacitance is not generated in the region where the plate electrode is buried. In other words, the parasitic capacitance is reduced by the height D of the concavity from the height of the

cell. The parasitic capacitance C_{p3} in this case is estimated by

$$C_{p3} = \varepsilon_0 \times \varepsilon_1 \times T_{s2} \times (H - D) \div T_{s1} \quad (7)$$

where D is the depth of the concavity in which the plate electrode is buried, T_{s1} is the distance between adjacent cells, T_{s2} is the long side length of the cell, and H is the height of the cell (see FIG. 6).

[0054]

Compared with the conventional example, the parasitic capacitance can be reduced by

$$\Delta C_{p3} = \varepsilon_0 \times \varepsilon_1 \times T_{s2} \times D \div T_{s1} \quad (8).$$

When the specific values in the conventional example are used and the depth D of the plate is 0.5 μm,

$$\Delta C_{p3} = 0.62 \text{ fF} \quad (9)$$

is obtained. This is 4.1% of the individual set cell capacitance value (15 fF). Accordingly, the parasitic capacitance, which is generated between a target capacitor and the capacitor adjacent to one side of the target capacitor, can be reduced by about 1.2%. In other words, this embodiment makes it possible to reduce the parasitic capacitance and suppress a signal error caused by noise, even if the desired cell size and capacitor size are set.

[0055]

It is preferable that the depth of the concavity in which the plate electrode is buried is set so that the value of the parasitic capacitance

between adjacent capacitors is not more than 10% of the set cell capacitance value.

[0056]

Other Embodiments

As described above, for the trench-type stacked structure, in which cell capacitors are formed without removing an interlayer insulating film, the parasitic capacitance is multiplied by a relative dielectric constant of the interlayer insulating film as a proportional constant. Therefore, it is particularly effective for the trench-type stacked cell capacitor structure to make the relative dielectric constant of the interlayer insulating film in which the cell capacitors are buried lower than the dielectric constant of a silicon oxide film.

[0057]

When the interlayer insulating film is a silicon oxide film (BPSG film) that includes 1 – 4% B (boron) and 4 – 8% P (phosphorus), the relative dielectric constant ε_2 is about 3.9. By using a so-called low dielectric constant film as the interlayer insulating film, the parasitic capacitance can be reduced proportionally.

[0058]

For example, when the interlayer insulating film is a silicon oxide film that includes F (fluorine) such as fluorosilicate glass (FSG), the relative dielectric constant is about 3.5. In this case, the parasitic capacitance value can be reduced by 3.5/3.9 times compared with the BPSG film.

[0059]

In addition to the silicon oxide film including F, examples of the low dielectric constant film that can be applied to the present invention include SiC, $SiC_xH_yO_z$ ($0 < x < 1$, $0 < y < 1$, and $0 < z < 2$), an amorphous carbon film,

other organic films and the like.

[0060]

When the method of this embodiment is used alone, it is preferable to use the interlayer insulating film having a relative dielectric constant that allows the capacitance between adjacent cell capacitors to be not more than 10% of the accumulated charge capacitance for each capacitor, specifically, a relative dielectric constant of 3.5 or less. This is because malfunction tends to occur when the relative dielectric constant is more than 10%.

[0061]

[Effects of the Invention]

The present invention can reduce the parasitic capacitance between adjacent capacitors and suppress a signal error caused by noise.

[Brief Description of the Drawings]

FIG. 1 shows a planar layout of a semiconductor device of the first embodiment of the present invention.

FIG. 2 is a cross-sectional view showing the structure of cell capacitors, taken along the line I–II in FIG. 1.

FIG. 3 shows a planar layout of a semiconductor device of the second embodiment of the present invention.

FIG. 4 is a cross-sectional view showing the structure of cell capacitors, taken along the line V–VI in FIG. 3.

FIG. 5 is a cross-sectional view showing a semiconductor device of the third embodiment of the present invention.

FIG. 6 is a top view showing trench-type stacked cell capacitors formed in a memory cell region.

FIG. 7 is a cross-sectional view showing the structure taken along the line I–II in FIG. 6.

FIG. 8 shows a storage capacity element portion (DRAM circuit).

FIG. 9 is a cross-sectional view showing the structure of simple-stacked memory cells.

FIG. 10 is a cross-sectional view showing the structure of cylindrical cell capacitors.

[Description of the Reference Numerals]

8	Storage node
9	Capacitor insulating film
10	Plate electrode
11	Interlayer insulating film
12	Plug
20a, b	Plate electrode
101	Storage node
102	Capacitor insulating film
103	Plate electrode
104	Storage node
105	Capacitor insulating film
106	Plate electrode
108a, 108b	Storage node
109	Capacitor insulating film
110	Plate electrode
111	Interlayer insulating film
112	Plug

[Name of the Document] ABSTRACT

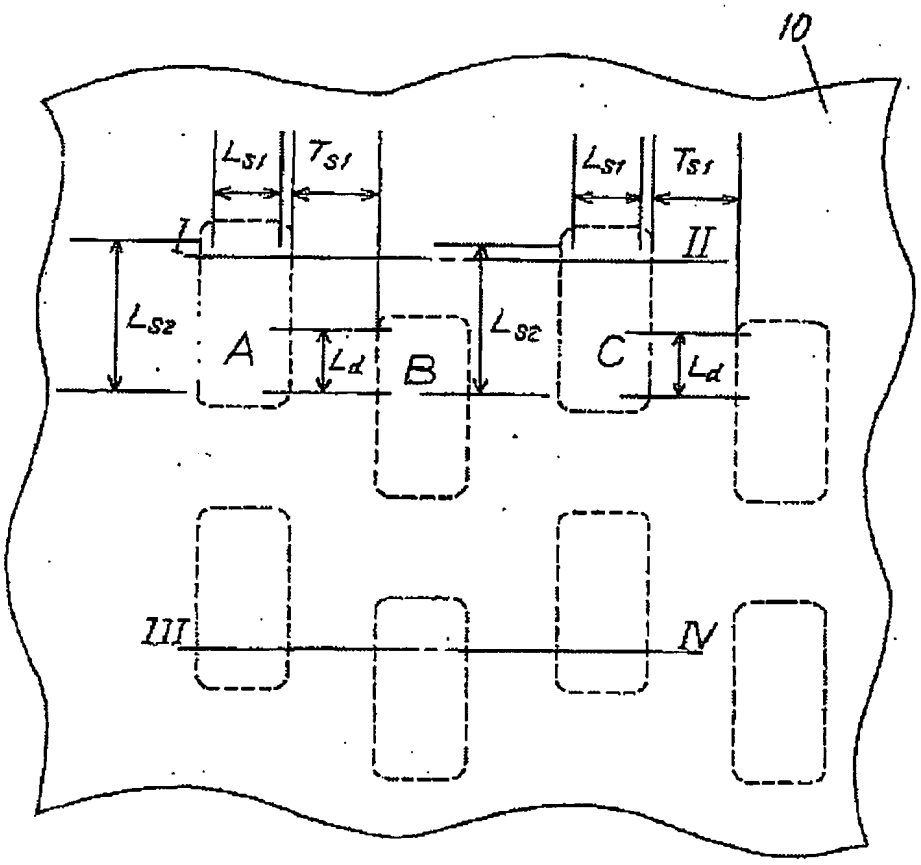
[Abstract]

[Objective] To provide a semiconductor device including a storage capacity element portion that can reduce a parasitic capacitance of DRAM memory cells having a trench-type stacked cell structure.

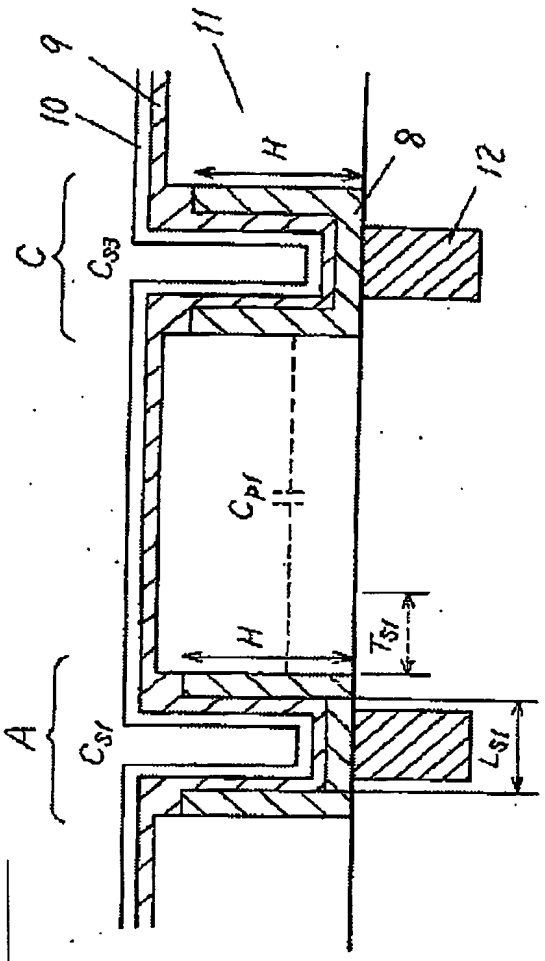
[Solution] The trench-type stacked cell structure includes many capacitors with the same shape. An interlayer insulating film 11 has a plurality of trenches, in each of which a storage node 8, a capacitor insulating film 9, and a plate electrode 10 are buried to form the capacitors. Any capacitor is arranged so that only a part of a side face of one trench is opposite to that of the other.

[Selected Figure] FIG. 2

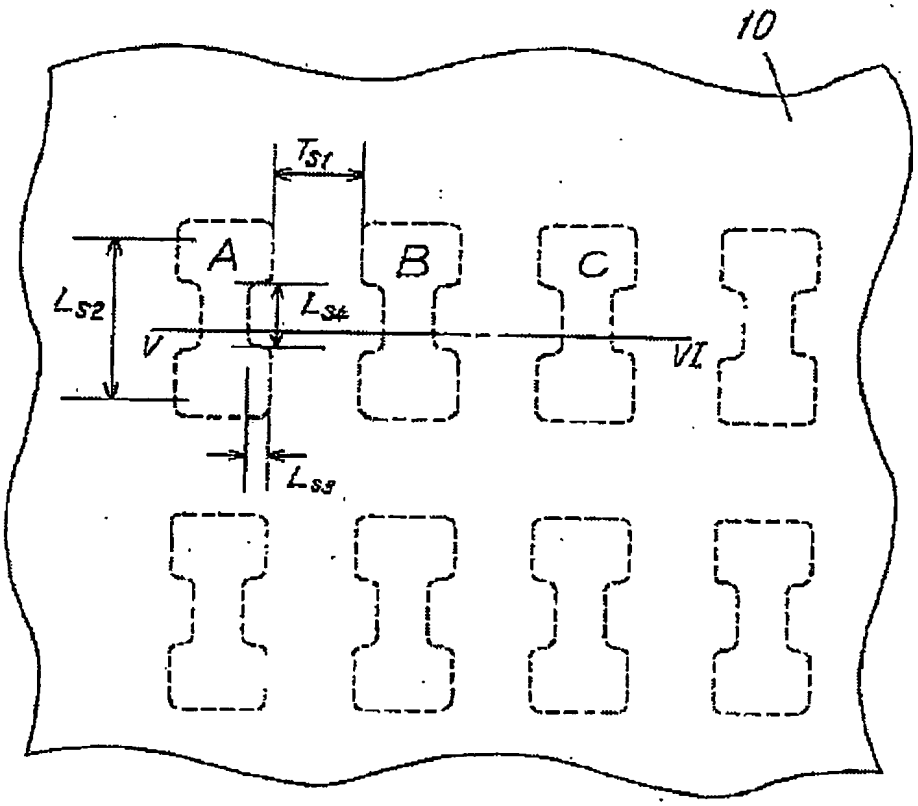
[Document Name] Drawings
[FIG. 1]



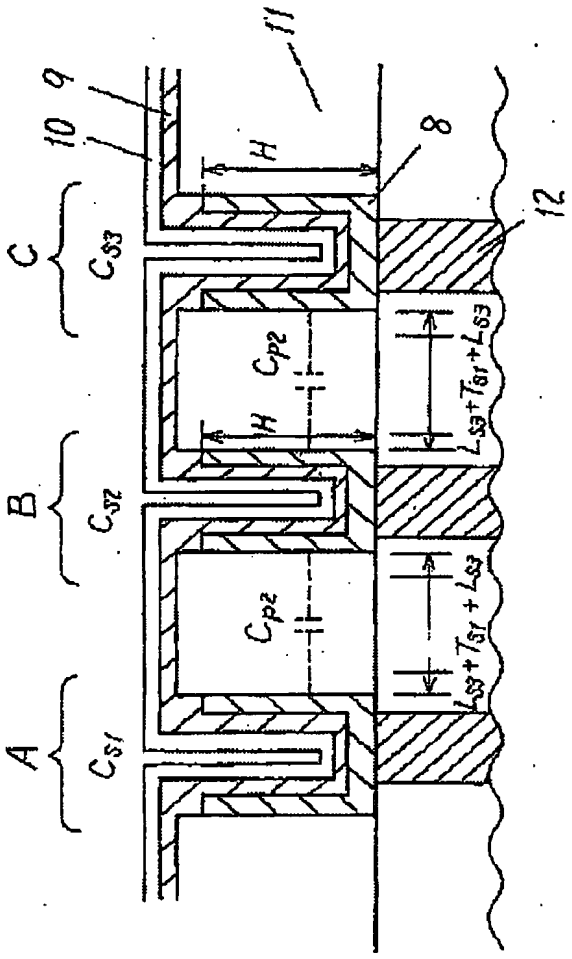
[FIG. 2]



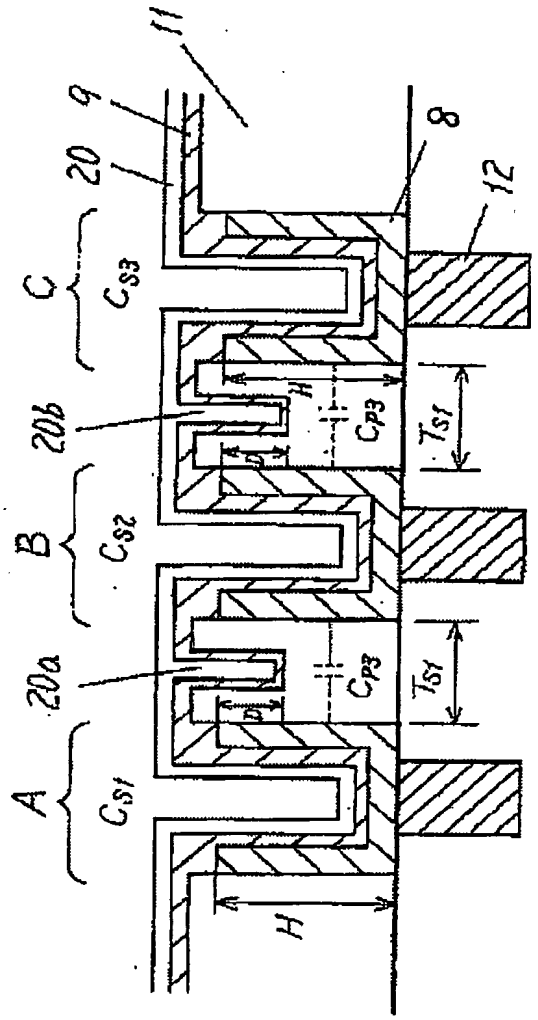
[FIG. 3]



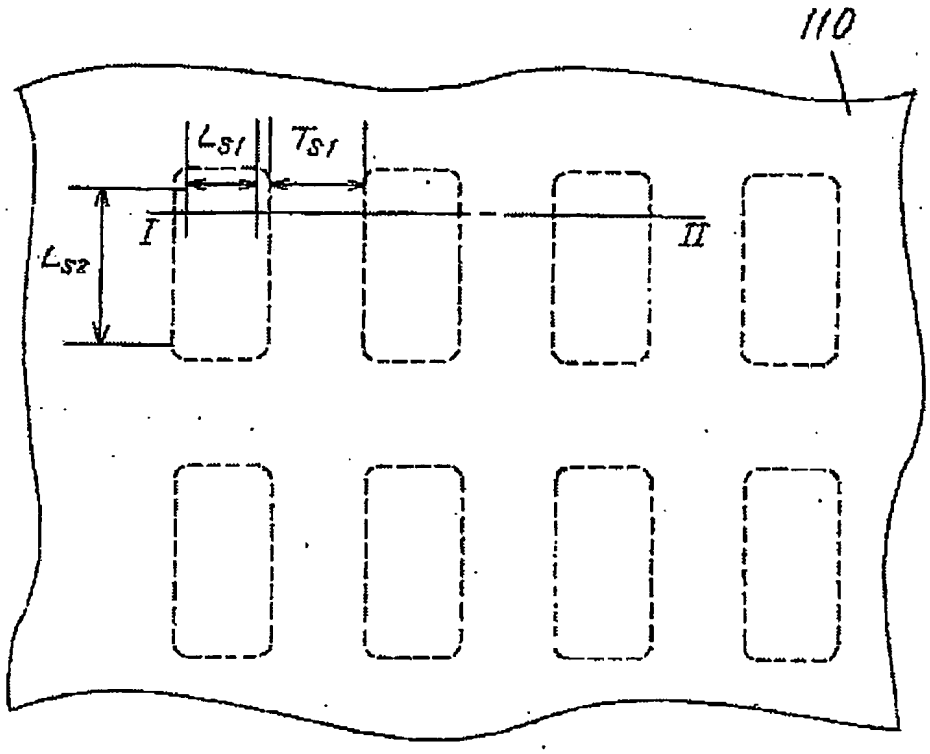
[FIG. 4]



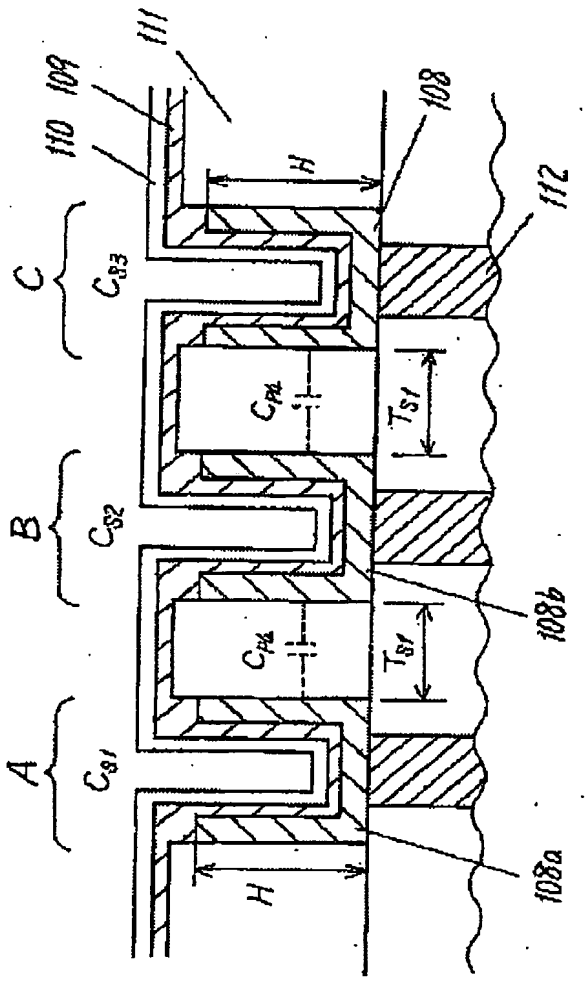
[FIG. 5]



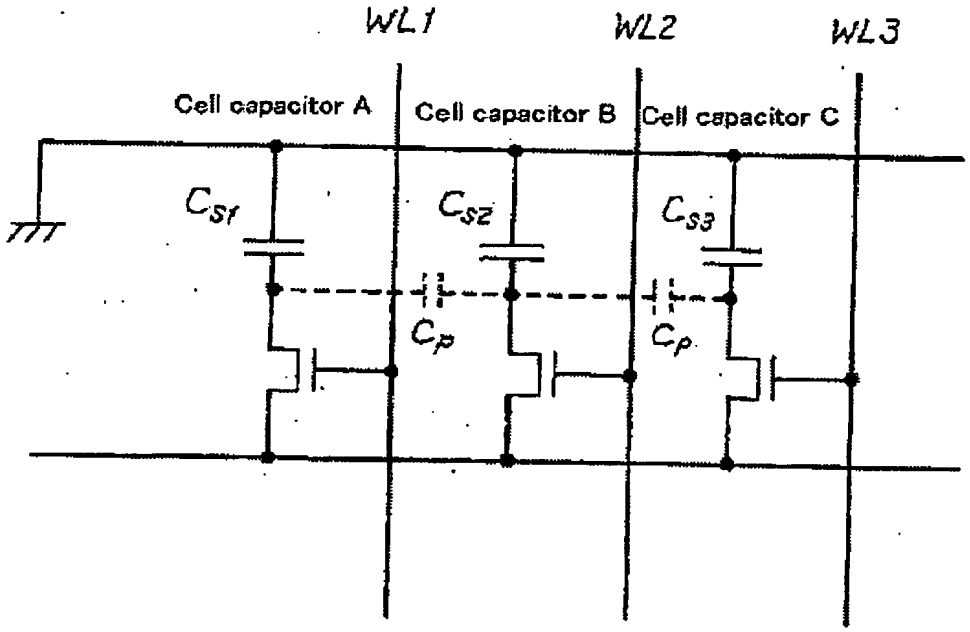
[FIG. 6]



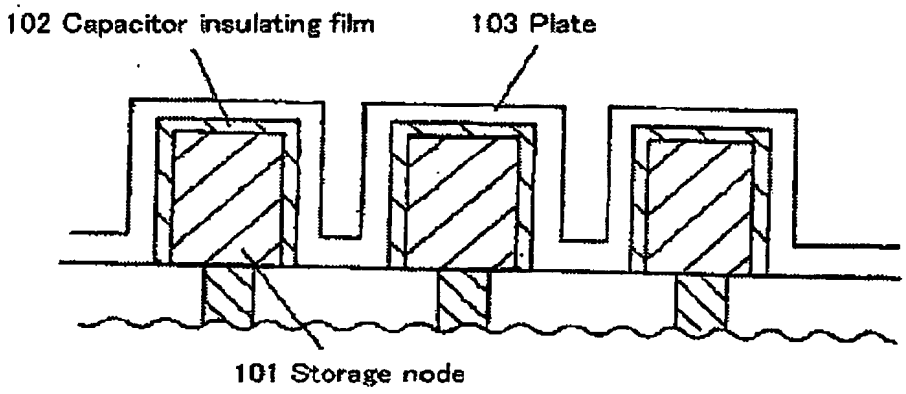
[FIG. 7]



[FIG. 8]



[FIG. 9]



[FIG. 10]